WHAT IS CLAIMED IS:

1. A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to an output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises:

first and second operational transconductance amplifiers (OTAs); and

a current mirror circuit, wherein

said first OTA receives said differential voltage; and

said second OTA has a first input terminal for receiving an output voltage from said first or second diode-connected transistor and has a second input terminal connected to an output terminal of said second OTA and driven with a current proportional to an output current of said first OTA, an output terminal voltage of said second OTA being said reference voltage.

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2. The CMOS reference voltage circuit as defined in claim 1 wherein the transconductance gm1 of said first OTA is equal to the transconductance gm2 of said second OTA (gm1 = gm2);

the current ratio of an input current to an output current in said current mirror circuit being set to 1:K2, where K2 > 1, to attain a desired amplification factor.

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3. The CMOS reference voltage circuit as defined in claim 1 wherein the current ratio of an input current to an output current in said current mirror circuit is 1:1; and wherein

the transconductance gm1 of said first OTA1 and that gm2 of said second OTA 2 are set so that

$$gm1 = K2 \times gm2, \text{ where } K2 > 1$$

to attain a desired amplification factor.

4. The CMOS reference voltage circuit as defined in claim 1 wherein the current ratio of an input current to an output current in said current mirror circuit is set to 1:K2, where K2 > 1; and wherein

the transconductance gm1 of said first OTA1 and the transconductance gm2 of said second OTA 2 are set so that

$$gm1 = K3 \times gm2, \text{ where } K3 > 1$$

to attain a desired amplification factor.

5. A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to an

output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises (K2+1) differential pairs, K2 being an integer not less than 1, wherein

the first differential pair receives said differential voltage;

one of differential pair transistors of the second differential pair receives an output voltage of the first or second diode-connected transistor, whilst the other of said differential pair transistors is diode-connected and is driven with a current proportional to an output current of one of the transistors of the first differential pair;

output voltages of diode-connected transistors of the second to number K2 differential pairs are applied to one of the differential pair transistors of the third to the number (K2+1) differential pairs, respectively, whilst the other transistors of the differential pair transistors are diode-connected and driven by currents proportional to the output current of the one transistor of the first differential pair;

the first to number (K2+1) differential pairs are driven with the (K2+1) constant currents bearing a predetermined constant current ratio relative to one another; and

the differential input voltages of the second to number (K2+1) differential pairs are summed together to produce an amplified voltage with a desired amplification factor.

6. A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively

grounded and driven by two constant currents with a constant current ratio; and

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means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to an output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises (K2+1) differential pairs, wherein

the first differential pair receives said differential voltage;

one of differential pair transistors of the second differential pair receives an output voltage of the first or second diode-connected transistor, whilst the other of said differential transistors is diode-connected;

the differential transistors of the third to number K2 differential pairs are diode-connected, a diode-connected differential transistor of a preceding stage and a diode-connected differential transistor of a subsequent stage being driven by constant currents with a predetermined constant current ratio K2;

the differential transistors of the number (K2+1) differential pairs are diode-connected, one diode-connected differential transistor being driven by a constant current along with the other diode-connected differential transistor of a preceding stage, the other diode-connected transistor being driven with the current proportional to the output current of said first differential pair;

the first to number (K2+1) differential pairs are driven with (K2+1) constant currents bearing a certain constant current ratio to one another; and

the differential input voltages of the second to number (K2+1) differential pairs are summed together to produce a desired amplification factor.

7. A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to an output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing is comprised of two differential pairs,

one of the differential transistors of a second one of said differential pairs receiving an output voltage of the first or second diode-connected transistors, the other differential transistor being diode-connected and being driven with a current proportional to an output current of one of the transistors of the first differential pair;

said first differential pair and the second differential pair being driven with two constant currents having a constant current ratio to each

other;

an operating input voltage range of said second differential pair being a predetermined number multiple of the operating input voltage range of said first differential pair to produce a desired amplification factor.

8. The CMOS reference voltage circuit as defined in claim 7 wherein the emitter area of said first diode-connected transistor is equal to the emitter area of said second diode-connected transistor, with the ratio of two constant currents not being equal to 1.

9. The CMOS reference voltage circuit as defined in claims 7 wherein the size of the first diode-connected transistor is K1 times the size of the second diode-connected transistor, with the driving current ratio not being equal to 1.

10. The CMOS reference voltage circuit as defined in claim 7 wherein the size of the first diode-connected transistor differs from the size of the second diode-connected transistor, with the driving current ratio being equal to 1.

11. The CMOS reference voltage circuit as defined in claim 7 wherein the gate W/L ratio of each transistor of said first differential pair is K2 times the gate W/L ratio of each transistor of said second differential pair, W and L being the gate width and the gate length of the transistor, respectively;

the driving current of said second differential pair being K3 times the driving current of said third differential pair; the output current of the first differential pair being multiplied by K3 to drive the diode-

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connected transistor of the second differential pair to produce the desired amplification factor.

12. A CMOS reference voltage circuit for generating and outputting a reference voltage, comprising:

a diode-connected transistor, having an emitter grounded and being driven with a constant current; and

an operational amplifier for receiving an output voltage of said diode-connected transistor, said operational amplifier being arranged in a voltage follower type configuration and having an input offset;

a reference voltage being output from an output terminal of said operational amplifier.

13. The CMOS reference voltage circuit as defined in claim 12 wherein

said operational amplifier is driven with a constant current;

the gate W/L ratio of two transistors constituting an input differential pair of said operational amplifier is 1:K2;

the gate W/L ratio of two transistors constituting an active load operating as a load to the two transistors of said input differential pair is K3:1; and

said offset of said operational amplifier is summed to said output voltage of said diode-connected transistor to produce said reference voltage.

14. The CMOS reference voltage circuit as defined in claim 12 wherein

said operational amplifier is driven with the constant current;

the gate W/L ratio of two transistors constituting an input differential pair is K2:1;

the gate W/L ratio of the two transistors constituting an active load operating as a load to the two transistors is 1:K3; and

said offset of said operational amplifier is subtracted from said output voltage of said diode-connected transistor to produce said reference voltage.

15. The CMOS reference voltage circuit as defined in claim 1 wherein

a diode is employed as said diode-connected transistor.

16. A reference voltage circuit, comprising

first and second emitter-grounded bipolar transistors, each having a base connected to a collector, with each collector being fed with a constant current;

first and second operational conductance amplifiers (OTAs), each having at least a first input terminal and a second input terminal and adapted for outputting from an output terminal a current proportional to a differential voltage between voltages applied to said first and second input terminals; and

a current mirror circuit having at least an input end and an output end, with the ratio of the current fed to said input end to the current output from the output end being of a predetermined value, wherein

the collectors of the first and second bipolar transistors are connected respectively to the first and second input terminals of the first OTA;

said output terminal of said first OTA is connected to said input end of said current mirror circuit;

the output terminal of said second OTA and said collector of said

second bipolar transistor are respectively connected to the first and second input terminals of said second OTA; and

a connection node of said first input terminal and the output terminal of said second OTA are connected to said output end of said current mirror circuit, said output terminal of said second OTA outputting a reference voltage.

17. The reference voltage circuit as defined in claim 16 wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the same constant current is supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor being of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor being of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor being of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor being of a value different from 1;

the differential voltage Δ VBE of the base-to-emitter voltages of said first and second bipolar transistors being of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the current ratio of said current mirror circuit being K2;

the values of transconductance of said first and second OTAs

being gm1 and gm2, respectively;

the reference voltage output from said output end of said second OTA being given by

$$VBE2 + \{K2 \times \Delta VBE2 \times gm1\}/gm2.$$

18. A reference voltage circuit comprising

first and second bipolar transistors, each having a emitter grounded and having a base connected to a collector, with each collector being fed with a constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common and driven with a constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a current mirror circuit having an input end and plural(K2) number of output ends, said current mirror circuit receiving from said input end an output current of said first differential pair and outputting output currents proportional to the input current at said plural (K2) number of output ends;

a second differential pair comprised of a pair of MOS transistors, having sources connected in common and driven with a constant current, one of the MOS transistors having a gate fed with a base-to-emitter voltage of said second bipolar transistor and the other MOS transistor having a gate connected to a drain and connected to the first output end of said current mirror circuit; and

third to number (K2+1) differential pairs, each comprised of a pair of MOS transistors, having sources connected in common and driven

with a constant current, one MOS transistor of said differential pair having a gate connected to a gate of a MOS transistor of a preceding stage differential pair having a drain connected to a gate, the other MOS transistor of said differential pair having a drain connected to a gate and connected to a corresponding output end of the current mirror circuit;

a reference voltage being taken out at a drain of the MOS transistor of the number (K2+1) differential pair having the drain and the gate connected together.

19. A reference voltage circuit comprising

first and second bipolar transistors, each having a emitter grounded and having a base connected to a collector, with each collector being fed with a constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a first current mirror circuit having an input end and an output end, said first current mirror circuit receiving from said input end an output current of said first differential pair and outputting output currents proportional to the input current at said output end;

a second current mirror circuit having an input end and plural(K2) number of output ends, said second current mirror circuit receiving from said input end a constant current from a constant current source and outputting output currents proportional to the input constant current at said K2 output ends;

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a second differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a constant current, one of the MOS transistors having a gate fed with a base-to-emitter voltage of said second bipolar transistor and the other MOS transistor having a gate connected to a drain and connected to the first output end of said current mirror circuit;

third to number K2 differential pairs, each comprised of a pair of MOS transistors, having sources connected in common driven with a constant current, each MOS transistor having a drain and a gate connected together, one MOS transistor of said differential pair, having a drain connected to a drain of the other MOS transistor of a preceding stage differential pair, said other MOS transistor having a drain and a gate connected together, said drain of said one MOS transistor being connected to the corresponding output end of the second current mirror circuit,

the other MOS transistor of said differential pair, having a drain connected to a drain of one MOS transistor of a subsequent stage differential pair, said one MOS transistor having a drain and a gate connected together, said drain of the other MOS transistor being connected to a corresponding output end of said second current mirror circuit; and

a number (K2+1) differential pair, each comprised of a pair of MOS transistors, having sources connected in common driven with a constant current, each MOS transistor having a drain and a gate connected together, the drain of one of the MOS transistors being

connected to the drain of the other MOS transistor of the number K2 differential pair having a drain and a gate connected together, said drain being connected to said output end of said first current mirror circuit, a reference voltage being taken out at the drain of the other MOS transistor as an output terminal.

20. The reference voltage circuit as defined in claim 18 wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the same constant current is supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; and wherein

the differential voltage Δ VBE of the base-to-emitter voltages of said first and second bipolar transistors is of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the reference voltage output from said number K2 differential pair being given by VBE2 + K2 $\times$ Δ VBE2.

21. A reference voltage circuit comprising:

first and second bipolar transistors, each having a emitter grounded and having a base connected to a collector, with each collector being fed with a constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a current mirror circuit having an input end and an output end, said input end being fed with an output current of said first differential pair and said output end outputting an output current corresponding to a preset proportion of the input current; and

a second differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a constant current, the gate of one of the MOS transistors being fed with a base-to-emitter voltage of said second bipolar transistor, the other MOS transistor having a drain and a gate connected together and connected to said output end of said current mirror circuit;

a reference voltage being taken out from the drain of the other MOS transistor of said second differential pair as an output terminal.

22. A reference voltage circuit including a differential amplifier circuit, said differential amplifier circuit comprising:

a differential pair comprised of first and second MOS transistors, having sources connected in common and driven with a constant current; and

a first current mirror circuit comprised of third and fourth MOS

transistors, connected to the drains of the first and second MOS transistors of said differential pair, said third and fourth MOS transistors acting as active loads, wherein

the gate W/L ratio of each of said first and second MOS transistors is 1:K2, with K2 being an integer larger than 1,

the gate W/L ratio of each of said third and fourth MOS transistors is K3:1, with K3 being an integer larger than 1; or

the gate W/L ratio of said first and second MOS transistors is K2:1, with the gate W/L ratio of said third and fourth MOS transistors being 1:K3; and

there is provided a bipolar transistor, having an emitter grounded and having a base and a collector connected together with the collector fed with a constant current; the collector of said bipolar transistor being connected to the gate of said first MOS transistor, a drain and a gate of the second MOS transistor being connected together, a reference voltage being taken out from the drain of said second MOS transistor as an output terminal.

23. The reference voltage circuit as defined in claim 22 comprising:

a fifth MOS transistor having a source grounded, a drain connected to one end of a resistor and having a gate coupled to the other end of said resistor;

a sixth MOS transistor having a source grounded and having a gate connected to the drain of said fifth MOS transistor; and

a second current mirror circuit having an input end and a plurality of output ends, said input end being connected to the drain of said sixth

MOS transistor and having said output ends connected to the common source of said first and second MOS transistors of said differential pair and to the collector of said bipolar transistor.

24. A reference voltage circuit including a differential amplifier circuit, said differential amplifier circuit comprising:

a differential pair comprised of first and second MOS transistors, having sources connected in common and driven with a constant current;

a first current mirror circuit comprised of third and fourth MOS transistors, connected respectively to the drains of the first and second MOS transistors of said differential pair, said third and fourth MOS transistors acting as active load; and

a fifth MOS transistor arranged in a source follower configuration, having a gate connected to the drain of the second MOS transistor and driven with a constant current, wherein

the gate W/L ratio of said first and second MOS transistors is 1:K2, where K2 being an integer larger than 1, with the gate W/L ratio of said third and fourth MOS transistors being K3:1, where K3 being an integer larger than 1; or

the gate W/L ratio of said first and second MOS transistors is K2:1, with the gate W/L ratio of said third and fourth MOS transistors being 1:K3;

a source of said fifth MOS transistor is an output terminal; said output terminal being connected to the gate of said second MOS transistor of said differential pair to form a voltage follower; and

there being provided a bipolar transistor, having an emitter

grounded and having a base and a collector connected together, with the collector being driven with a constant current;

the collector of said bipolar transistor being connected to the gate of said first MOS transistor of said differential pair;

a reference voltage being taken out at said output terminal.

25. The reference voltage circuit as defined in claim 24 comprising:

a sixth MOS transistor having a source grounded, a drain connected to one end of a resistor and having a gate connected to the other end of said resistor;

a seventh MOS transistor having a source grounded and having a gate connected to a drain of said sixth MOS transistor; and

a second current mirror circuit including one input end and a plurality of output ends, having the input end connected to the drain of the seventh MOS transistor and having the output end connected to the drain of said sixth MOS transistor, the source of said fifth MOS transistor, the common source of the first and second MOS transistors of said differential pair and to the collector of said bipolar transistor.

26. The reference voltage circuit as defined in claim 16 comprising a cathode-grounded diode in place of said emitter-grounded bipolar transistor, having the base and the collector connected together.

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20. The reference voltage circuit as defined in claim 19 wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the same constant current is supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the

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emitter area of the second bipolar transistor is of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; and wherein

the differential voltage Δ VBE of the base-to-emitter voltages of said first and second bipolar transistors is of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the reference voltage output from said number K2 differential pair being given by VBE2 + K2 $\times$ Δ VBE2.